UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	044204-0308162	5788

27498 7590 10/31/2006

PILLSBURY WINTHROP SHAW PITTMAN LLP
P.O. BOX 10500
MCLEAN, VA 22102

EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED
OCT 3 1 2006
Technology Center 2100

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/847,991
Filing Date: May 02, 2001
Appellant(s): KIM ET AL.

Anthony G. Smyth
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/7/06 appealing from the Office action mailed 11/09/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,636,933	MacLellan et al	10-2003
5,053,942	Srini	10-1991
5,081,575	Hiller et al	1-1992

6,125,429	Goodwin et al	9-2000
5,394,551	Holt et al	2-1995
5,805,030	Dhuey et al	9-1998

Microsoft Press Computer Dictionary second and third editions: Definitions of Priority and Semaphore.

Structured Computer Organization: Shows that hardware and software are logically equivalent.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 8-9, 11-13, 18-19, 21-22 and 24-25 are rejected under 35 U.S.C. 103(e) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551.

As per claims 1, 11 and 24, Goodwin discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 12), comprising: one or more processors (CPU0 to CPU3); one

or more resources (memory M0-M3 or I/0 16) capable of being shared by the one or more processors (CPU0-CPU3); and a resource controller (arbitor 14) and bus (X-bar 12) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 2, lines 46-52; col. 4, lines 26-36; 49-62). Goodwin et al does not expressly teach the operation of the arbiter including a semaphore. Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claims 2, 8, 12, 18 and 25, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 3, 9, 13 and 19, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

As per claim 21, Goodwin discloses an apparatus for controlling the access to one or more memory resources by one or more processors, the controller comprising a memory resource controller (arbitor 14) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62).

As per claim 22, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

3. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551 as applied to claim 1 and further in view of what is well known in the art as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, Goodwin teaches all the limitations of the claimed invention including crossbar switch. However, Goodwin is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 6 and 16, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

4. Claim 27 is rejected under 35 U.S.C. 103(e) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of what is well known in the art as evidenced by Dhuey et al PN 5,805,030.

As per claim 27, Goodwin discloses a computer system (10; fig. 1) comprising: a first processor (20); a second processor (22); a multipath memory controller (arbitor 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62); a multipath peripheral controller (arbitor 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of peripheral resources and a second bus that is capable of connecting the second processor to the same set of peripheral resources wherein the first and second processors are capable of simultaneously accessing different peripheral resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource. Goodwin in view of Holt teaches a single resource controller with semaphores for each resource. Official Notice is taken that to have separate Memory controller and Peripheral controllers is well known in the art. See for example Dhuey et al Figure 1 items 30 and 40. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have separate memory and peripheral controllers because this would have allowed for faster concurrent access processing of different types of resources. See also MPEP 2144.04 V. C.

5. Claims 1-3, 8-9, 11-13, 18-19, 21-22, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLellan et al PN 6,636,933 in view of Holt et al PN 5,394,551.

As per claims 1,11, and 21, MacLellan discloses a computer system (100) having a multipath cross bar bus (crossbar 5004), comprising: one or more processors (121); one or more resources (memory 220 see figs 8B, 9A-9C) capable of being shared by the one or more processors (121); and a resource controller and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource(within 220) from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources within 220 from different processors; parallel transfers or simultaneous accesses; col. 14, line 35 to col. 15, line 5; col. 18, lines 50-53; col. 20, line 58 to col. 21, line 2). MacLellan also teaches semaphores for signaling however MacLellan is silent as to how the Semaphores are to be implemented. Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claims 2 and 12, MacLellan discloses memory resources (plural global memory boards 220; col. 12, lines 41+; Fig. 8; col. 14, lines 12+ to col. 15, lines 1+); memory controller (logic sections e.g. 5010; col. 18, lines 42-55);

As per claims 3, 13 and 22, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

As per claims 8, 18 and 24, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 9, 19 and 25, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+).

6. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable MacLellan et al (USPN 6,636,933; MacLellan) in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of what is well known in the art as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, MacLellan teaches all the limitations of the claimed invention including crossbar switch. However, MacLellan is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is

capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 6 and 16, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

7. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacLellan et al PN 6,636,933 in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of what is well known in the art as evidenced by Dhuey et al PN 5,805,030.

As per claim 27, MacLellan discloses a computer system (100; fig. 1) comprising: a first processor (121_1); a second processor (121_2); a multipath memory controller having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2); a multipath peripheral controller having a first bus that is capable of connecting the first processor to a set of peripheral resources (disk drives) and a second bus that is capable of connecting the second processor to the same set of peripheral resources (disk drives) wherein the

first and second processors are capable of simultaneously accessing different peripheral resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource. MacLellan in view of Holt teaches a single resource controller with semaphores for each resource. Official Notice is taken that to have separate Memory controller and Peripheral controllers is well known in the art. See for example Dhuey et al Figure 1 items 30 and 40. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have separate memory and peripheral controllers because this would have allowed for faster concurrent access processing of different types of resources. See also MPEP 2144.04 V. C.

8. Claims 1-3 are rejected under 35 U.S.C. 103(b) as being unpatentable over Srini (USPN 5,053,942) in view of Holt et al PN 5,394,551.

As per claim 1, Srini discloses a computer system (e.g. Fig. 1) having a multipath cross bar bus (crossbar matrix 20), comprising: one or more processors (12); one or more resources (memory 22) capable of being shared by the one or more processors (12); and a resource controller (crossbar chip 10) and bus (26) that is connected to each resource and to each

processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 8, lines 30-50). Srini does not expressly teach a semaphore. Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claim 2, Srini discloses memory resources (plural memory modules 22; col. 4, lines 15+); memory controller (arbiter 18 and logic; col. 4, lines 41-51);

As per claim 3, Srini discloses crossbar switches 20; and resource arbitration controller (arbiter 18; col. 4, lines 41+)

9. Claims 1-2, 11-12, 21 and 24 are rejected under 35 U.S.C. 103(b) as being unpatentable over Hiller et al. (USPN 5,081,575; Hiller) in view of Holt et al PN 5,394,551.

As per claims 1, 11 and 24, Hiller discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 6), comprising: one or more processors (PEs); one or more resources (PMEMs 8) capable of being shared by the one or more processors (PEs); and a resource controller (control section Column 2 line 3-9) and bus (crossbar switch) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 6, lines 55-57). Hiller teaches all access cycles taking the same time there is no need for arbitration. Holt et al teaches each resource of a plurality of shared resources has a

semaphore which controls access to the shared resource (Column 2 lines 59-68) that are accesses in an overlapping manner. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would allowed for longer memory accesses such as burst cycles etc.. by preventing multiple concurrent accesses of the same shared resource.

As per claims 2 and 12, Hiller discloses memory (PMEMs 8); memory controller (control section; col. 6, lines 55 et seq).

As per claim 21, Hiller discloses an apparatus for controlling the access to one or more memory resources (PMEMs) by one or more processors (PEs), the controller comprising a memory resource controller (control section; col. 6, lines 55 et seq) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 6, lines 55-57).

10. Claims 3-4, 13-14, 22-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable Hiller et al. (USPN 5,081,575; Hiller) in view of in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of Goodwin et al. (USPN 6,125,429; Goodwin).

As per claims 3, 13, 23 and 25; Hiller discloses crossbar switch 6. However, Hiller does not teach an arbitration controller. Goodwin teaches that it is known to use a resource arbitration controller to resolve contentions or collisions in a computer system using a crossbar switch (col. 2, lines 30-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hiller and Goodwin as taught by Goodwin to

include a resource arbitration controller in a crossbar switch type system such as that of Hiller to resolve the collisions and contentions particularly in bus systems such as that of Hiller with large numbers of data users (PEs) and resources (PMEMs) connected to them (col. 2, lines 55-67).

As per claims 4, 14, 23 and 26, Hiller teaches that the crossbar switch comprises multiplexer (col. 6, lines 57-64).

(10) Response to Argument

At the outset in considering the claim language the examiner notes that the claim language includes "one or more processors" interacting with "one or more resources" and thus the claim scope encompasses one processor interacting with one either a single resource or a plurality of resources as well as a plurality of processors interacting with either a single resource or a plurality of resources. Although applicant argues a narrower interpretation of the claim language, the plain meaning of the claim language involved is broader than applicants interpretation and applicant has not amended claim language during prosecution to require the narrower interpretation argued thus in evaluation patentability of the claims over the prior art the examiner has relied upon the broader interpretation consistent with the claim language as presented.

Further in regards to the breadth of the claim language. The claim language requires a semaphore. The examiner has included two dictionary definitions of semaphore showing that a semaphore is simply some indication of whether a shared resource is in use for controlling access to a shared resource and that the purpose of a semaphore is to help maintain order among competing processes for the shared resource.

Response to arguments regarding Goodwin

In regards to applicants argument that Goodwin is directed to different subject matter in which a hardware semaphore unit for controlling access is of no consequence: While it is true that Goodwin's invention is directed to cache coherency, this has no bearing on the fact that the system in which Goodwin solves the cache coherency problem also teaches a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 12), comprising: one or more processors (CPU0 to CPU3); one or more resources (memory M0-M3 or I/0 16) capable of being shared by the one or more processors (CPU0-CPU3); and a resource controller (arbitor 14) and bus (X-bar 12) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 2, lines 46-52; col. 4, lines 26-36; 49-62).

In regards to applicants argument that the operation of the arbiter chip is not the subject of Goodwin's disclosure and is not described further: The examiner thanks the applicant for pointing out that Goodwin is silent upon how the arbiter handles contention in accessing the shared resources. Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have allowed the arbiter to prevented multiple concurrent accesses of the same shared resource.

Response to arguments regarding MacLellan

In the final rejection the examiner provided two separate mappings of the claim language to MacLellan et al. Applicants arguments have made clear that the scope of the claims coverage excludes reading the claim language on the disk drives of MacLellan. Therefore the alternative mapping of the claims "one or more resources" to MacLellan et al's disk drives is withdrawn in the rejection as stated above. The breadth of the claim terminology still encompasses the mapping in the rejection of the "one or more resources" to MacLellan et al's memories 220.

In regards to applicants argument that MacLellan does not teach or suggest a resource controller capable of permitting one or more processors to simultaneously access different resources: For clarity of applicants argument the applicants specification makes clear that while one processor accesses one resource a second processor simultaneously accesses a different resource. As oppose to one processor simultaneously accessing different resources. MacLellan clearly teaches a resource controller that allows one or more processors within 120 (see figures 8B-9C) to access one or more resources (Memory boards within memory 220 each board being divided into separate memory regions fig 8C (Just like applicants separate portions see applicants specification Page 6 line 25 to Page 7 line 7)) while a second processor within 120 simultaneously accesses a different resource or even the same memory board but a different region within the board. See Column 14 line 35 to Column 15 line 5; Col 18 line 50-53; and Col 20 line 58 to Col 21 line 2.

In regards to applicants argument that the directors 180 control the data transfer: The applicant is correct. The examiner may have pointed to the wrong item as the controller. This

does not alleviate the fact that MacLellan teaches controlling simultaneous accesses from a plurality of processors to different ones of a plurality of resources whether the resources be taken as disk drives or memory boards within a cache. Whatever controls this function is the controller.

In regards to applicants argument that the processors and disk drives of MacLellan are connected indirectly through cache 220 and that the message network 260 is merely a conduct for communication between directors: Applicant have already pointed to the section in MacLellan that teaches the back end directors $200_1 - 200_{32}$ are mapped to the disk drives. And front end directors are mapped to the processors. The examiner recognizes that there are two different types of accesses. There are messages which are between the front end directors to the back end directors. And there is data transfers from the processors via the front end directors to the cache memory boards.

Since the applicants have not addressed the mapping of the memories 220 to the claimed "one or more resources" the rejection to MacLellan should be maintained.

In regards to applicants argument that the examiner alleges that a superficial reference to data communication semaphores in MacLellan provides sufficient motivation for a skilled artisan to combine MacLellan with Holt : MacLellan teaches semaphores. The motivation and purpose of semaphores is to preventing multiple concurrent accesses of the same shared resource is a well known problem in systems with shared resources. MacLellan however is silent as to how the semaphores should be implemented. Holt teaches the use of hardware semaphores to solve this problem. The fact that MacLellan mentions semaphores is just a bonus in that there is no need for MacLellan to even mention semaphores since Holt expressly teaches the use of a hardware

semaphore for the purpose of preventing multiple concurrent accesses to the same shared resource.

In regards to applicants argument that MacLellan never teaches of suggests semaphores for controlling access to shared resources: That is the purpose of a semaphore. See the dictionary definition of semaphore.

In regards to applicants argument that MacLellan never teaches or suggests a *hardware* semaphore unit: the examiner agrees. Holt teaches a method of implementing semaphores. MacLellan only suggests that semaphores are used without any indication as to how they are to be implemented. A person of ordinary skill in the art at the time of the invention would have been motivated to look at Holt for a teaching of how to implement the semaphores.

Response to arguments regarding Srini

In regards to applicants argument that Srini is silent regarding the use of semaphores: The examiner agrees. Holt teaches the use of semaphores.

In regards to applicants argument that Srini discloses arbitration using arbiter cells implemented as a Mealy Machine using J-K flip flops. In Srini the arbitration scheme operates to select between requesters in a manner that ensures by switching access between requesters in successive cycles. Thus Srini's arbitration includes forces alteration of access rights between successive cycles: The examiner agrees. Srini also provides an acknowledgement to the requester when it is granted access. The requester does not always get granted access sometimes the memory is busy (See Column 4 lines 1-10). Srini is silent as to what mechanism is to be used to implement this busy control if the memory is busy. The purpose of semaphores is to

prevent contention by for controlling access to shared resources. A semaphore uses a flag to indicate the resource is busy. Holt et al teaches a method of implementing hardware semaphores. A person of ordinary skill in the art at the time of the invention mould have been motivated to look at Holt et al for a method of indicating the memory is busy.

In regards to applicants argument that Srini is directed to a crossbar switch that provides individual connections for processors and memory. Srini teaches a system that prevents more than one processor from accessing the same memory module: It is noted that the features upon which applicant relies "more than one processor accessing the same memory" module is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The examiner further notes in accordance with the applicants own specification, more than one processor cannot access the same resource (M1 or M2 or M3 or M4) at the same time unless applicant decides to redefine the resource as the group of all the memories. If applicants are defining all memories M1-M4 as a single resource then likewise the group of all memory modules 22 of Srini are defined as a single resource.

In regards to applicants argument that the examiner is wrong in indicating Srini does not state how it knows which resource is in use, that Srini's arbitration requires knowledge of which requester is using each resource and that the arbitration taught by Srini explicitly predicated on such awareness: The examiner notes that this is the definition of semaphores see dictionary definition of semaphore. The examiner reviewed the section cited by applicant and while the examiner accepts applicants contention that Srini teaches a hardware semaphore as claimed the section cited appeared only to indicate which requester was granted access to a resource and

allow fairness as opposed to an indication of which resource is in use. If, as applicants have argued, Srini teaches the claimed semaphore then Srini should have been applied as a 102 however the examiner was unable to find an express statement in Srini that Srini's arbiter includes an indication of which resource is in use therefore the 103 rejection is maintained in that is clearly obvious to include an indication of which resource is in use as applicants have argued.

Response to arguments regarding Hiller

In regards to applicants argument that Hiller and Holt do not render obvious a resource controller that includes a hardware semaphore unit for controlling access to shared resources: this is clearly incorrect. While it is true that Hillers reconfiguring the connections each access cycle eliminates the need for arbitration. This limits all accesses to be of the same length or to cause the entire system to wait until every access is done before a new configuration (See column 6 line 65 to Column 7 line 8). It would have been obvious to include a semaphore to indicate which memory is in use when reconfiguring because this would have allowed for accesses of differing lengths such as burst etc...

Response to general arguments

In regards to applicants argument that the examiner suggests that hardware and software are logically equivalent and relies on this suggestion in rejecting the claims. However, the examiner cites no art that teaches the implementation of a hardware semaphore unit. Nor does the examiner articulate a reason that a skilled artisan would have been motivated to alter the cited

art to implement a semaphore unit in hardware: This is clearly false. In the final rejection the applicant argued that Holt was not a hardware unit. The following was the examiners response

> "Holt's semaphore unit is expressly a mechanism/unit. However for the sake of argument hardware and software are logically equivalent. Thus, even if Holt's did not expressly state the semaphore was a mechanism/unit. It would have been obvious to a person of ordinary skill in the art to use a hardware semaphore in the system of MacLellan in view of Holt because this would have provided for one of the well known purposes of using hardware (such as hardware is faster than software)."

The examiner then cited in the final rejection "Structured Computer Organization: Shows that hardware and software are logically equivalent." To support the examiners statement. That hardware and software are logically equivalent and that hardware is faster than software.

In regards to applicants argument that the examiner has not given due consideration to relative clocking speeds of processor and speculative hardware semaphore unit (e.g. internal clock v. peripheral bus speed) that could have easily allowed a processor to implement a faster software semaphore scheme: Yes the examiner did consider these clock speeds etc. The examiner notes none of the cited references teach different clock speeds. And all things being equal i.e. the hardware and software using the same clock hardware is faster than software.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

PRM

Paul R. Myers
PAUL R. MYERS
PRIMARY EXAMINER

Conferees:

***

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER